Ramin Bashizade – Curriculum Vitae

Sharif University of Technology, Azadi Ave.,
Tehran, Iran
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Research Interests

- Networks-on-Chip
- Memory System and Cache Design for CMPs and GPUs

Education

M.Sc. in Computer Architecture *2011-2013*
***Sharif University of Technology**, Tehran, Iran*
Thesis Title: A Fully-Pipelined Reconfigurable Router Microarchitecture for on-Chip Routers
Under the supervision of Prof. Hamid Sarbazi-azad
GPA: 17.09/20

B.Sc. in Computer Engineering *2007-2011*
***Shahed University**, Tehran, Iran*
Thesis Title: A University Timetabling Program Using Local Search Algorithms
Under the supervision of Prof. Maryam Hasanzadeh
GPA: 16.31/20 (Last Year GPA: 18.33/20)

Awards and Honors

- Ranked 2nd in the first National Digital Design Contest – I was the head of *H.A.L. 9000* team (Implementing a Blokus Duo player on an FPGA board – Among 62 participating teams, and 6 finalists) *2013*
- Ranked 2nd in the National PhD Entrance Exam - Computer Architecture (Among 605 examinees) *2013*
- Ranked 25th in the National M.Sc. Entrance Exam - Computer Architecture (Among approximately 20,000 examinees – did not enroll) *2011*

Teaching Experience

Digital Design Course Teaching Assistant (Under the supervision of Prof. Shaahin Hessabi), *Sharif University of Technology, Tehran, Iran* *Spring 2013*

Electrical Circuits Lab. Teaching Assistant (Under the supervision of Prof. Afshin Hemmatyar), *Sharif University of Technology, Tehran, Iran* *Summer 2014*

Publications

- Sadrosadati M., **Bashizade R.**, Shafiee A., Sarbazi-azad H., "A General Method to Improve Adaptivity of Turn Model Based Routing Algorithms in Mesh NoCs" (To Be Submitted to TVLSI)

- Samavatian M.H., Arjomand M., **Bashizade R.**, Sarbazi-azad H., "Architecting the Last-Level Cache for GPUs Using STT-RAM Technology" (Submitted to TODAES)
- **Bashizade R.**, Sarbazi-azad H., "Traffic-Aware Buffer Reconfiguration in on-Chip Networks", *DAC 2015* (Submitted)
- **Bashizade R.**, Sarbazi-azad H., "P2R2: Parallel Pseudo-Round-Robin Arbiter for High-Performance Networks-on-Chip", *INTEGRATION, the VLSI Journal* (Accepted, to Be Published)
- **Bashizade R.**, Hasanzadeh M., "Optimizing University Course Timetable Using Local Search Methods", *Soft Computing Journal*, vol. 2, no. 1, pp. 24-31, Spring-Summer 2012, Kashan, Iran. (In Persian)

Employment

- **Network Engineer – Part Time**, *Darya Co., Tehran, Iran* — *Sept. 14' – present*
  Implementing a NAS System for Home and Small Office Applications
- **Software Engineer – Part Time**, *Amin Software Co., Tehran, Iran* — *Oct. 13' - Aug. 14'*
  Working with MATLAB, MySQL and C++ Programming
- **Research Assistant**, *Institute for Research in Fundamental Sciences (IPM), Tehran, Iran* — *Sept. 13' – present*
  Doing Research on NoCs and GPU Cache

Standard Tests

TOEFL iBT: 101 (Reading: 26, Listening: 30, Speaking: 23, Writing: 22)

GRE: Verbal Reasoning: 158, Quantitative Reasoning: 170, Analytical Writing: 4.0

Skills

Programming Languages and HDLs: C/C++, C#, SQL, Verilog

Tools: Synopsys Design Compiler, Synopsys SoC Encounter, ModelSim, MATLAB, ISIS Proteus, Xilinx ISE, Altera Quartus II, Synopsys TetraMAX, gem5 Full-System Simulator, GPGPU-Sim

References

- Hamid Sarbazi-azad
  Professor at Computer Engineering Dept.
  Sharif University of Technology, Tehran, Iran
  Email: azad@sharif.edu
- Shaahin Hessabi
  Associate Professor at Computer Engineering Dept.
  Sharif University of Technology, Tehran, Iran
  Email: hessabi@sharif.edu
- Maryam Hasanzade
  Assistant Professor at Engineering Dept.
  Shahed University, Tehran, Iran
  Email: hasanzadeh@shahed.ac.ir