Pejman Lotfi-Kamran **October 2014**

CONTACT INFORMATION

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RESEARCH INTERESTS

Computer architecture. More specifically, I am interested in cross-stack and technology-driven innovations for improving performance and energy efficiency of computer systems for emerging applications including big data.

EMPLOYMENT

- **Postdoctoral Researcher.** Institute for Research in Fundamental Sciences (IPM) Jul. 2014

EDUCATION

- **Ph.D. in Computer Science.** Swiss Federal Institute of Technology in Lausanne (EPFL) Sep. 2013
  Advisor: Prof. Babak Falsafi
  Thesis: *Scale-Out Processors*
- **M.S. in Electrical and Computer Engineering.** University of Tehran Feb. 2005
  Advisor: Prof. Zainalabedin Navabi
  Co-Advisor: Prof. Mehran Massoumi
  Thesis: *An Efficient Data Structure for RTL Representation*
  GPA: 18.78/20.00 (graduated with honors)
- **B.S. in Electrical and Computer Engineering.** University of Tehran Sep. 2002
  Advisor: Prof. Zainalabedin Navabi
  Thesis: *Implementation of a VHDL-AMS-to-CHIRE compiler*
  GPA: 17.40/20.00 (graduated with honors)

HONORS AND AWARDS

- **Intel Ph.D. Fellowship Award.** 2012-2013 Academic Year 2012
- **Paper Award** from the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) for "NOC-Out: Microarchitecting a Scale-Out Processor" 2012
- **Paper Award** from the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) for "Scale-Out Processors" 2012
- **Paper Award** from the School of Computer and Communication Sciences at EPFL for "Cuckoo Directory: A Scalable Directory for Many-Core Systems" 2011
- **Paper Award** from the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) for "Cuckoo Directory: A Scalable Directory for Many-Core Systems" 2011
- **Best Student Paper Finalist** at the 17th International Symposium on High Performance Computer Architecture (HPCA) for "Cuckoo Directory: A Scalable Directory for Many-Core Systems" 2011
- **Best Paper Award** from the 13th Iranian Conference on Electrical Engineering for "Improving Logic-Level Representation of BMD/TED Diagrams" 2005
- **Dean's Honored Graduate.** College of Engineering, University of Tehran 2002
  Ranked 3^{rd} among all students who graduated in 2002
- **Faculty of Engineering (FOE) Award.** University of Tehran, Computer Engineering track 2002
  Annually awarded to the top three students in each track by College of Engineering
- **Ranked 8^{th}** among 5,445 participants of Iran's national M.S. entrance exam. Computer Engineering track 2002

- **Ranked 2**nd among 50 computer engineering graduated students of the 1998 class 2002
- **Ranked 11**th among 30,000 participants of Iran's Region 3 B.S. entrance exam. Mathematics and Physics track 1998

PUBLICATIONS **Conference Papers**

1. **P. Lotfi-Kamran**, B. Grot, and B. Falsafi, "NOC-Out: Microarchitecting a Scale-Out Processor," in *International Symposium on Microarchitecture (MICRO)*, pp. 177–187, December 2012.
2. D. Milojevic, S. Idgunji, D. Jevdjic, E. Ozer, **P. Lotfi-Kamran**, A. Panteli, A. Prodromou, C. Nicopoulos, D. Hardy, B. Falsafi, and Y. Sazeides, "Thermal Characterization of Cloud Workloads on a Power-Efficient Server-on-Chip," in *International Conference on Computer Design (ICCD)*, pp. 175–182, October 2012.
3. **P. Lotfi-Kamran**, B. Grot, M. Ferdman, S. Volos, O. Kocberber, J. Picorel, A. Adileh, D. Jevdjic, S. Idgunji, E. Ozer, and B. Falsafi, "Scale-Out Processors," in *International Symposium on Computer Architecture (ISCA)*, pp. 500–511, June 2012.
4. M. Hosseinabady, **P. Lotfi-Kamran**, J. Mathew, S. Mohanty, and D. Pradhan, "Single-Event Transient Analysis in High Speed Circuits," in *International Symposium on Electronic System Design (ISED)*, pp. 112–117, December 2011.
5. M. Ferdman, **P. Lotfi-Kamran**, K. Balet, and B. Falsafi, "Cuckoo Directory: A Scalable Directory for Many-Core Systems," in *International Symposium on High Performance Computer Architecture (HPCA)*, pp. 169–180, February 2011. (**Selected by the program committee for the best student paper session**)
6. **P. Lotfi-Kamran**, M. Ferdman, D. Crisan, and B. Falsafi, "TurboTag: Lookup Filtering to Reduce Coherence Directory Power," in *International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 377–382, August 2010.
7. A.-M. Rahmani, I. Kamali, **P. Lotfi-Kamran**, A. Afzali-Kusha, and S. Safari, "Negative Exponential Distribution Traffic Pattern for Power/Performance Analysis of Network on Chips," in *International Conference on VLSI Design (VLSID)*, pp. 157–162, January 2009.
8. **P. Lotfi-Kamran**, M. Daneshtalab, C. Lucas, and Z. Navabi, "BARP–A Dynamic Routing Protocol for Balanced Distribution of Traffic in NOCs," in *Design, Automation and Test in Europe (DATE)*, pp. 541–546, March 2008.
9. **P. Lotfi-Kamran**, A.-A. Salehpour, A.-M. Rahmani, A. Afzali-Kusha, and Z. Navabi "Stall Power Reduction in Pipelined Architecture Processors," in *International Conference on VLSI Design (VLSID)*, pp. 541–546, January 2008.
10. **P. Lotfi-Kamran**, M. Massoumi, M. Mirzaei, and Z. Navabi, "Enhanced TED: A New Data Structure for RTL Verification," in *International Conference on VLSI Design (VLSID)*, pp. 481–486, January 2008.
11. M. Hosseinabady, M. H. Neishaburi, **P. Lotfi-Kamran**, and Z. Navabi, "A UML Based System Level Failure Rate Assessment Technique for SoC Designs," in *VLSI Test Symposium (VTS)*, pp. 243–247, May 2007.
12. M. Hosseinabady, **P. Lotfi-Kamran**, G. Di Natale, S. Di Carlo, A. Benso, and P. Prinetto, "Single-Event Upset Analysis and Protection in High Speed Circuits," in *European Test Symposium (ETS)*, pp. 29–34, May 2006.
13. M. Hosseinabady, **P. Lotfi-Kamran**, P. Riahi, F. Lombardi, and Z. Navabi, "A Flow Graph Technique for DFT Controller Modification," in *International System-on-Chip Conference (SOCC)*, pp. 55–60, September 2005.
14. A. Hooshmand, S. Shamshiri, M. Alisafaee, B. Alizadeh, **P. Lotfi-Kamran**, M. Naderi, and Z. Navabi, "Binary Taylor Diagrams: An Efficient Implementation of Taylor Expansion Diagrams," in *International Symposium on Circuits and Systems (ISCAS)*, vol. 1, pp. 424–427, May 2005.
15. **P. Lotfi-Kamran**, H. Shojaei, H. Parandeh-Afshar, M. Naderi, and Z. Navabi, "Improving Logic-Level Representation of BMD/TED Diagrams," in *Iranian Conference on Electrical Engineering (ICEE)*, pp. 448–453, May 2005. (**Recognized as best paper by the program committee**)
16. **P. Lotfi-Kamran**, M. Hosseinabady, H. Shojaei, M. Massoumi, and Z. Navabi, "TED+: A Data Structure for Microprocessor Verification," in *Asia South Pacific Design Automation Conference (ASP–DAC)*, vol. 1, pp. 567–572, January 2005.

Journal Papers

1. B. Grot, D. Hardy, **P. Lotfi-Kamran**, B. Falsafi, C. Nicopoulos, and Y. Sazeides, "Optimizing Data-Center TCO with Scale-Out Processors," in *IEEE Micro, Special Issue on Energy-Aware Computing*, vol. 32, no. 5, pp. 52–63, September/October 2012.
2. **P. Lotfi-Kamran**, A.-M. Rahmani, M. Daneshtalab, A. Afzali-Kusha, and Z. Navabi, "EDXY–A Low-Cost Congestion-Aware Routing Algorithm for Network-on-Chips," in *Elsevier Journal of Systems Architecture – Embedded Systems Design (JSA–ESD)*, vol. 56, no. 7, pp. 256–264, July 2010.
3. M. Hosseinabady, **P. Lotfi-Kamran**, F. Lombardi, and Z. Navabi, "Low Overhead DFT Using CDFG by Modifying Controller," in *IET Computers & Digital Techniques (IET–CDT)*, vol. 1, no. 4, pp. 322–333, July 2007.
4. M. Hosseinabady, **P. Lotfi-Kamran**, and Z. Navabi, "Low Test Application Time Resource Binding for Behavioral Synthesis," in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 12, no. 2, article 16, April 2007.
5. **P. Lotfi-Kamran** and Z. Navabi, "Improving Logic-Level Representation of Taylor Expansion Diagram Using Attributed Edges," in *Iranian Journal of Science and Technology (IJST), Transaction B, Technology*, vol. 30, no. B6, pp. 735–748, 2006.

Workshop & Poster Papers

1. S. Idgunji, D. Milojevic, E. Ozer, **P. Lotfi-Kamran**, D. Jevdjic, and B. Falsafi, "Performance and Efficiency of 3D-Stacked DRAM in a Multicore System," in *Workshop on 3D Integration – Applications, Technology, Architecture, Design, Automation and Test in Conjunction with Design, Automation and Test in Europe (DATE)*, March 2012.
2. E. Ozer, K. Flautner, S. Idgunji, A. Saidi, Y. Sazeides, B. Ahsan, N. Ladas, C. Nicopoulos, I. Sideris, B. Falsafi, A. Adileh, M. Ferdman, **P. Lotfi-Kamran**, M. Kuulusa, P. Marchal, and N. Minas, "EuroCloud: Energy-Conscious 3D Server-on-Chip for Green Cloud Services," in *Workshop on Architectural Concerns in Large Datacenters in Conjunction with International Symposium on Computer Architecture (ISCA)*, June 2010.
3. M. Hosseinabady, **P. Lotfi-Kamran**, and Z. Navabi, "Controller-Aware Hierarchical Test Generation and Testability Analysis," in *European Test Symposium (ETS)*, May 2005.
4. M. Alisafaee, **P. Lotfi-Kamran**, S. Shamshiri, H. Esmaeilzadeh, A. Pedram, and Z. Navabi, "MCBIST: A New Online BIST Scheme," in *Workshop on RTL and High Level Testing (WRTLT)*, pp. 85–90, November 2004.
5. M. Hosseinabady, **P. Lotfi-Kamran**, A. Pedram, and Z. Navabi, "A Binary Wavelet Test Compression," in *Workshop on RTL and High Level Testing (WRTLT)*, November 2004.
6. S. Shamshiri, H. Esmaeilzadeh, M. Alisafaee, **P. Lotfi-Kamran**, and Z. Navabi, "Test Instruction Set (TIS): An Instruction Level CPU Core Self-Testing Method," in *European Test Symposium (ETS)*, May 2004.

Research Experience

- **postdoctoral researcher.** *School of Computer Science* — Jul. 2014–date
  Institute for Research in Fundamental Sciences (IPM)
- **Research assistant.** *Parallel Systems Architecture (PARSA) Lab* — Sep. 2008–Sep. 2013
  Swiss Federal Institute of Technology in Lausanne (EPFL)
  Advisor: Babak Falsafi

Organization of Scale-Out Processors. *I proposed NOC-Out, a many-core organization for Scale-Out Processors that has low area overhead and provides fast access to the last-level cache (LLC) for delivering high performance. Today's many-core organizations force a compromise between performance and cost. Thus, many-core organizations based on a mesh interconnect have a modest area and wire cost, yet incur latency overheads through a many-hop topology. In contrast, many-core organizations based on richly connected topologies, such as a flattened butterfly, offer low latency at high area and wire cost. While existing many-core organizations offer an uneasy compromise between low area overhead and fast access to the LLC, NOC-Out offers both features simultaneously. The proposed organization is based on one simple and critical observation: there is almost no core-to-core communication in scale-out workloads. Based on this observation, this organization decouples cores and the last-level cache, eliminates all unneeded core-to-core links, and uses specialized core-to-LLC networks to connect cores to the last-level cache and vice versa. The bottom line is that NOC-Out delivers the performance of the state-of-the-art many-core organization with 1/10th of the area [MICRO'12].*

Scale-Out Processors. *I proposed a methodology for the design of highly efficient many-core processors for scale-out workloads. This research relies on two critical observations with regard to such many-core processors. First, large LLCs waste precious silicon real estate that could have been better used to integrate more cores. Second, the organization of a many-core processor has a significant impact on its performance. Existing many-core chips, such as those offered by Tilera, sacrifice much of the on-die real estate to LLC and employ a tiled organization that incurs a high on-chip communication overhead. In contrast, I proposed a many-core processor based on the notion of pods. A pod is a module that tightly couples many cores to a modestly sized LLC through a low-latency interconnect. The proposed processor integrates many pods wherein each pod is a self-contained server-on-a-chip running a full software stack. I formulated a methodology to determine the optimal number of cores and LLC capacity to integrate in a pod for peak throughput. The proposed design, called the Scale-Out Processor, delivers peak throughput in today's process technology and affords near-ideal scalability as the technology scales [ISCA'12].*

Area- and Energy-Efficient Coherence Directories for Many-Core CMPs. *We proposed the Cuckoo directory, an energy- and area-efficient scalable directory organization. Existing directory organizations suffer from the lack of energy or area efficiency at high core counts due to wide associative lookups or capacity overprovisioning. The Cuckoo directory, however, scales to high core counts without the energy costs of wide associative lookup and without gross capacity overprovisioning. The Cuckoo directory borrows heavily from Cuckoo Hashing, a dense-storage software hashing technique. Rather than significantly over-provisioning storage capacity to avoid storage conflicts in a traditional lookup table, the Cuckoo directory uses the Cuckoo Hashing algorithm to relocate conflicting entries within the directory to alternate non-conflicting locations. Leveraging the mathematically robust properties of Cuckoo Hashing enables compact and energy-efficient coherence directories with predictable asymptotic behavior and without degenerate cases, improving the state-of-the-art directory design without increasing complexity [HPCA'11].*

Lookup Filtering to Reduce Power Consumption of Coherence Directories. *To reduce the energy usage of coherence directories in many-core processors, I proposed the TurboTag filtering mechanism. Coherence directories dissipate a significant fraction of their power on unnecessary lookups when running commercial server and scientific workloads. These workloads have large working sets that are beyond the reach of on-chip caches of modern processors. Limited to capturing a small part of the working set, private caches retain cache blocks only for a short period of time before replacing them with new blocks. Moreover, coherence enforcement is a known performance bottleneck of multi-threaded software; hence, data sharing in optimized high-performance software is minimal. Consequently, the majority of the accesses to the coherence directory find no sharers in the directory because the data are not available in the on-chip private caches, effectively wasting power on the coherence checks. TurboTag reduces power consumption of coherence directories by filtering (almost all) needless directory lookups [ISLPED'10].*

CloudSuite Workloads. *CloudSuite is a benchmark suite for emerging scale-out applications. To enable full-system simulation of CloudSuite benchmarks, we brought up CloudSuite workloads on Flexus, our in-house, full-system simulator. I led the effort on bringing up CloudSuite workloads. We released the workloads to the broader research community.*

Flexus Full-System Simulator. *Flexus is a family of component-based C++ computer architecture simulators that enable full-system, timing-accurate simulation of uni- and multi-processor systems running unmodified commercial applications and operating systems. I contributed to the development of Flexus and also served as the coordinator of its mailing list.*

- **Research assistant.** *Computer-Aided Design (CAD) Lab* Jul. 2002–Aug. 2008
  University of Tehran
  Advisor: Zainalabedin Navabi

Cost-Effective Globally Aware Dynamic Routing Protocols to Avoid Congestion in NOCs. *I proposed low-cost adaptive routing algorithms for network-wide congestion avoidance. This research enhanced conventional adaptive routings that only rely on local indicators for congestion estimation with low-cost, non-local (global) indicators [DATE'08, JSA–ESD'10].*

Statistical Analysis for Soft Error Rate Estimation. *The effect of Single-Event Transients (SETs) on the system reliability is a big concern for ICs manufactured using advanced technologies. An SET in the combinational part of a circuit may propagate as a transient pulse to the input of a flip-flop and, consequently, gets latched, thus generating a soft error. Using the Probability Density Function (PDF) of an SET, we proposed a statistical method to compute the probability of soft errors considering dynamic behavior of a circuit [ETS'06, ISED'11].*

Low-Overhead Controller-Aware Design for Test. *We proposed a low-cost design for test (DFT) that requires minor modifications to the controller of digital systems. In this research, we took advantage of existing data paths in digital systems to provide controllability and observability for the test process. Furthermore, we introduced additional data paths by altering states or adding new transitions in the controllers of digital systems. The proposed DFT considerably reduces the test application time by ignoring unnecessary control states in the test process [IET–CDT'07].*

Low Test Application Time Test Synthesis. *Increased density and the need to test for new types of defects in nanometer technologies have resulted in a tremendous increase in test application time. We presented a test synthesis mechanism to reduce test application time for testing the datapath of a digital system. The reduction in the test application time was achieved by applying a test time-aware, resource-sharing algorithm on a scheduled control data flow graph of a design [TODAES'07].*

Data Structure for Efficient RT-Level Representation. *Formal verification of microprocessors requires a mechanism for efficient representation and manipulation of both arithmetic and random Boolean functions. State-of-the-art representations can effectively represent arithmetic expressions at the word-level but are not memory efficient in representing bit-level logic expressions. In this research, I presented modifications to the state-of-the-art representations to improve the ability of bit-level logic representation while maintaining robustness in arithmetic word-level representation [ASP–DAC'05].*

VHDL-AMS Analyzer. *VHDL-AMS is a derivative of the hardware description language VHDL that includes analog and mixed-signal extensions (AMS) in order to define the behavior of analog and mixed-signal systems. I developed an analyzer to compile VHDL-AMS to CHIRE, our in-house intermediate format.*

Teaching Experience

- **Instructor.** Designed course, gave lectures, held office hours, answered email/newsgroup queries, designed and graded homework and exams.

CE723: Advanced Computer Architecture. Sharif University of Technology	Spring 2014–Fall 2014
ECE061: Discrete Mathematical Structures. University of Tehran	Spring 2007–Spring 2008
Operating Systems. University of Tehran, IT education series for professionals with no computer science background.	Spring 2003

- **Teaching assistant.** Held office hours, answered email/newsgroup queries, led review sessions, designed and graded student homework.

CS471: Advanced Multiprocessor Architecture. EPFL	Fall 2009 and Fall 2012
CS198: Information Technology Project. EPFL	Fall 2011
ECE367: Digital Logic Circuits. University of Tehran	Spring 2004–Spring 2005
ECE354: Telecommunications 1. University of Tehran	Fall 2003–Spring 2004
ECE046: Microprocessors Lab. University of Tehran	Spring 2003
ECE207: Microprocessors. University of Tehran	Spring 2002

Professional Activities

- **Reviewer.**

International Symposium on High Performance Computer Architecture (HPCA)	2014
IEEE Transactions on Computers (TCOM)	2014
Elsevier Journal of Computer and System Sciences (JCSS)	2014
ACM Transactions on Embedded Computing Systems (TECS)	2013
International Symposium on High Performance Computer Architecture (HPCA)	2013
ACM Transactions on Architecture and Code Optimization (TACO)	2012
International Symposium on Microarchitecture (MICRO)	2012
Elsevier Journal of System Architecture (JSA)	2012

- **Member.**
  - ACM and ACM SIGARCH — Nov. 2008–date
  - IEEE and IEEE Computer Society — Jan. 2005–date

Tutorials

- **CloudSuite on Flexus.**
  - CSICC 2013, Tehran, Tehran, Iran — Mar. 2013
  - ISCA 2012, Portland, Oregon, USA — Jun. 2012
- **Flexus.**
  - IISWC 2010, Atlanta, Georgia, USA — Dec. 2010

Work Experience

- **Senior Design Engineer.** Public Switched Telephone Network (PSTN) Branch, Parstel Information and Telecommunication Technology Co. Inc. — Dec. 2005–Aug. 2008
- **Design Engineer.** Programmable Logic Controller (PLC) Branch, Arman Optimized Systems — Jun. 2001–Feb. 2002